

M.Winter on behalf of the IReS-LEPSI (and coll.) R&D teams

Outline

► **Introductory remarks:**

- important fabrication parameters
- summary of prototypes fabricated since 1999

► **Results and potential of the sensors:**

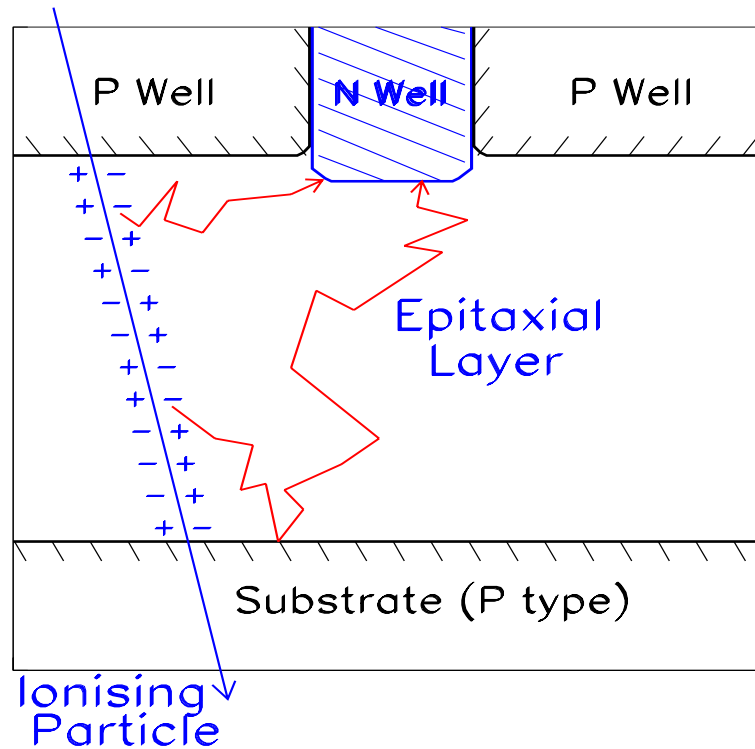
- spatial resolution
- material budget
- read-out speed
- radiation tolerance

► **Plans for 2003**

- sensor and its r.o. architecture
- integration in vertex detector

Fabrication parameters

► Principle of Operation:



► Requirements:

- ◇ thickness of epitaxial layer should be $> 5 \mu m$
- ◇ nb of metal layers should be > 3
- ◇ fabrication feature size should be $\lesssim 0.35 \mu m$
- ◇ fabrication process should be analog

⇒ **Exploration of fabrication process
is still an important task**

Summary of prototypes fabricated

► 6 MIMOSA prototypes fabricated since 1999

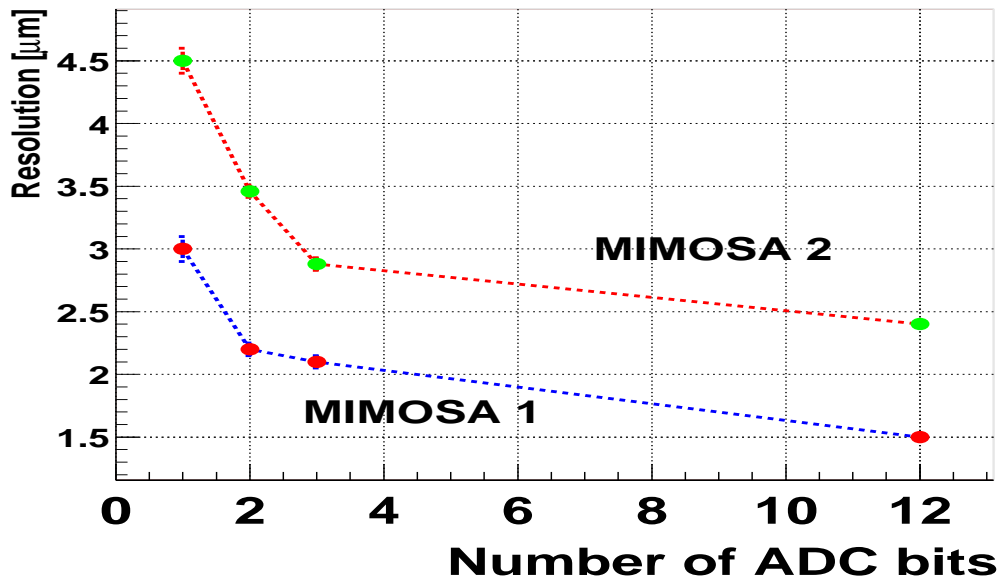
chip	year	process	epi.	pitch	metal	peculiar
M1	1999	AMS $0.6\mu m$	$14\mu m$	$20\mu m$	3M	thick epitaxy
M2	2000	MIETEC $0.35\mu m$	$4.2\mu m$	$20\mu m$	5M	thin epitaxy
M3	2001	IBM $0.25\mu m$	$2\mu m$	$8\mu m$	3M	deep sub-μm
M4	2001	AMS $0.35\mu m$	0 !	$20\mu m$	3M	low dop. substrate
M5	2001	AMS $0.6\mu m$	$14\mu m$	$17\mu m$	3M	real scale
M6	2002	MIETEC $0.35\mu m$	$4.2\mu m$	$28\mu m$	5M	col. // r.o. int. spars.

► **MIMOSA-1, -2, -3, -4, -5 tested**
(in particular with $120 \text{ GeV/c } \pi^-$ at CERN-SPS)

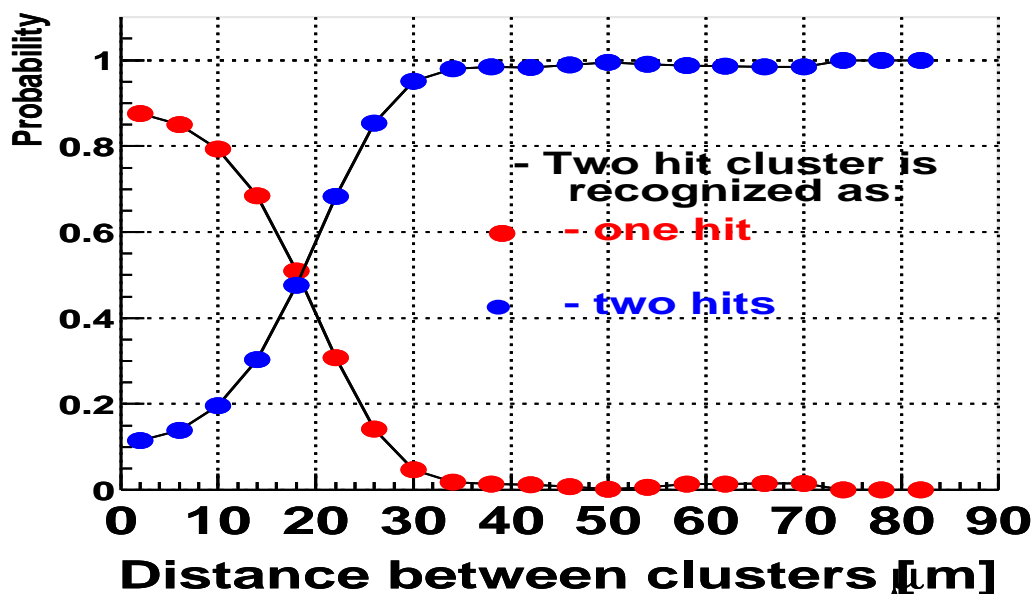
► **MIMOSA-6: tests starting now**

Spatial resolution

- ▶ $\sigma_{sp} \sim 1.5$ (2.2) μm with 14 (4) μm epitaxial layer
 ↳ is $\lesssim 2 \mu m$ necessary ? (will be investigated in 2003)
- ▶ single point resolution as a function of ADC-bit encoding:
 $\sigma_{sp} \sim 2$ -2.5 μm for 3 bits (~ 3 -4 μm for 1 bit ...)



- ▶ double track resolution: excellent down to 30 μm distance



► chip thickness:

- ◇ 120 μm works already with MIMOSA-5 (3.5 cm² chip)
- ◇ 80 μm under way with MIMOSA-5
- ◇ \lesssim 50 μm under devt (results expected in March 2003)

► stitching:

- ◇ industry standard: \lesssim 1 μm band between chips
- ◇ production yield of chips is crucial to make ladders

► mechanical support:

- ◇ depends on stitching possibility
- ◇ alternative designs under study (with their csq on physics)

► cooling:

- ◇ not needed in principle
- ◇ but may help reducing S/N

(\Rightarrow more integrated functionalities, better $\sigma_{sp,2tr}$)

- ◇ data treatment inside pixel may produce P_{diss} of

up to a few 100 μW /pixel during pixel read-out (only !)

\Rightarrow using at least part (1/10 ?) of collider duty cycle is crucial

\hookrightarrow switch on/off tests of MIMOSA-5 & estimates of

max. $\overline{P_{diss}}$ without heavy cooling planned in 2003

Read-out speed

► single pixel $f_{r.o.} \gtrsim 50$ MHz achievable

⇒ 2 cm long columns of 10^3 pixels can be read-out in $\lesssim 20 \mu s$

BUT signal treatment inside pixel requires several clock cycles

⇒ $\lesssim 50 \mu s$ ladder r.o. time needs to be demonstrated

↪ non trivial data flux reduction problem

(as for any of the technologies considered)

► on the other hand, full signal treatment at chip periphery
may not be the optimal solution because it suffers from the
dispersion of pixel characteristics

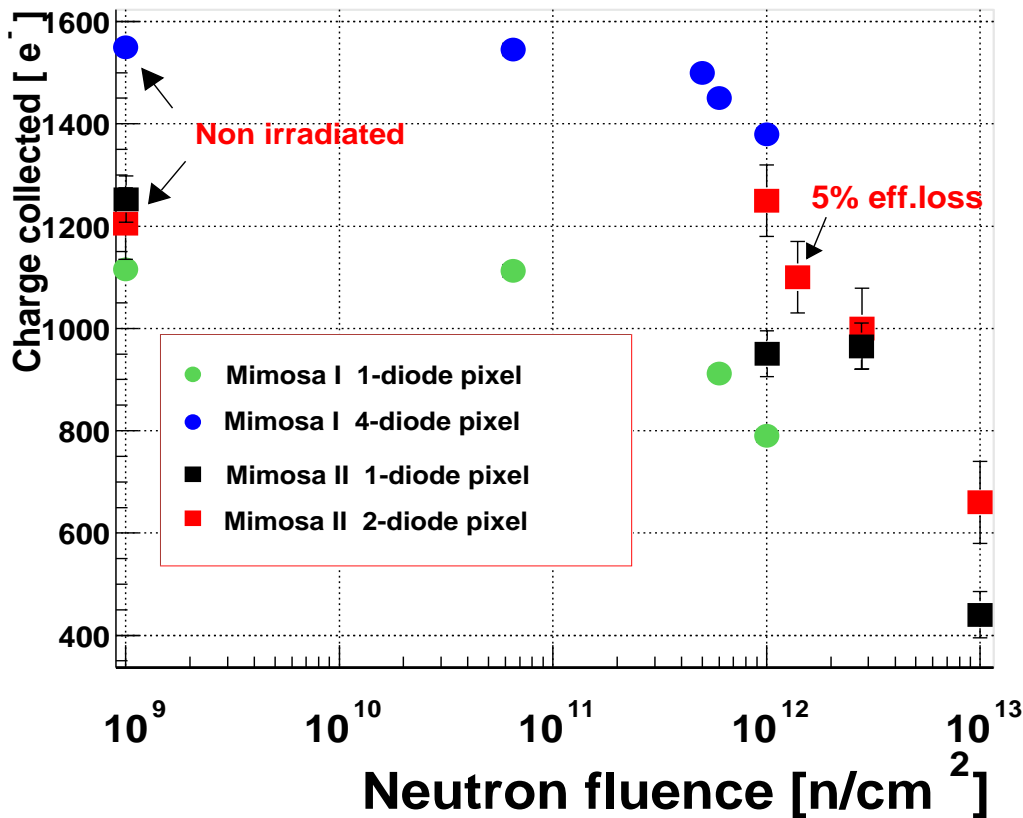
► natural choice to ensure high frame r.o. speed:
group pixels in (short) columns perpendicular to beam dir.

BUT: ◇ passive surface hosting col. r.o. μ circuits inside V_{fid}

◇ (presumably) substantial P_{diss} inside V_{fid}

⇒ question/optimum will be investigated in 2003

► Neutrons (irradiation of up to $10^{13} \text{ n}_{eq}/\text{cm}^2$):



◇ modest increase of leakage current / noise observed ($\lesssim 10\%$)
 \Rightarrow fluences of $\lesssim 10^{12} \text{ n}_{eq}/\text{cm}^2$ acceptable

► Ionising radiation:

- ◇ few 100 kRad acceptable
- ◇ better if $T \ll 0^\circ\text{C}$ (?)
- ◇ exact source(s) of performance loss under investigation

► Ccl: radiation tolerance at a FLC should not be an issue

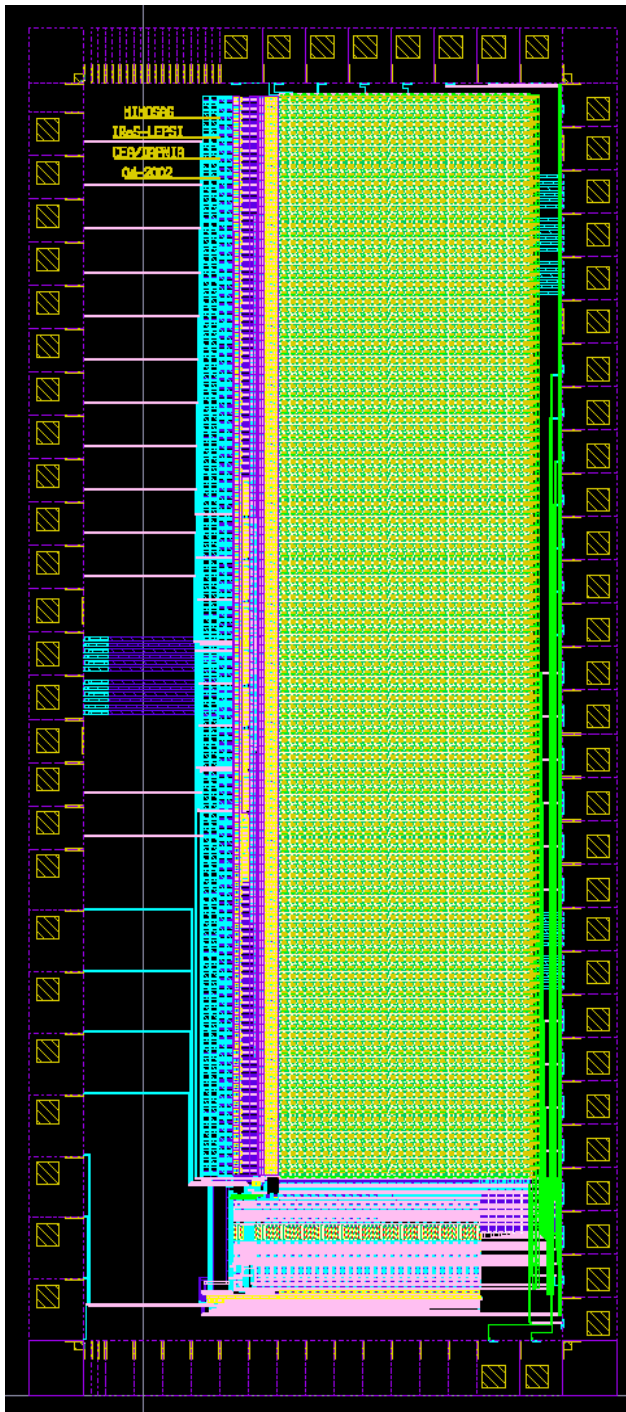
- ▶ **test MIMOSA-6: column // read-out with data treatment**
micro-circuits integrated inside pixels and on chip periphery
(see next transp. →)
- ▶ **design successor of MIMOSA-6 (larger surface ?)**
- ▶ **continue exploring fabrication processes:**
 - ◇ **0.25 μm TSMC (8 μm epitaxial layer)**
 - ◇ **0.35 μm AMS (8 μm epitaxial layer)**
- ▶ **continue investigating potential of MIMOSA-4 fab. process**
(0.35 μm AMS: no epitaxial layer but low doping substrate)
- ▶ **achieve $\lesssim 50 \mu m$ thinning on real scale chip (MIMOSA-5)**
- ▶ **work on tolerance to ionising radiation (not really for FLC)**

--- 00000 ---

- **design first DAS circuits**
- **study various versions of mechanical support (with/without stitching) and evaluate the influence of their mat. budget on the measurement performances of physics processes (e.g. $t\bar{t}H$)**
- **evaluate average P_{diss} :**
detector simulations, switch off/on tests with MIMOSA-5
- **continue studies based on physics processes aiming for the best compromise between granularity, r.o. speed and mat. budget**

MIMOSA-6 global layout

► 1st sensor with sparsification integrated / substrate:



- amplification (x5.5) and noise suppression (CDS) on pixel
- discriminator integrated on chip periphery (1 per column)

♣ 0.35 μm MIETEC technology
(same process as MIMOSA-2)

♣ 30 columns read-out in $\downarrow\downarrow$:

- 128 pixels per column
- 30 MHz r.o. frequency
- 6 clock cycles per pixel

⇒ 5 MHz effective r.o. frequency

◁ $P_{diss} \sim 500 \mu W$ per column
and frame r.o. cycle

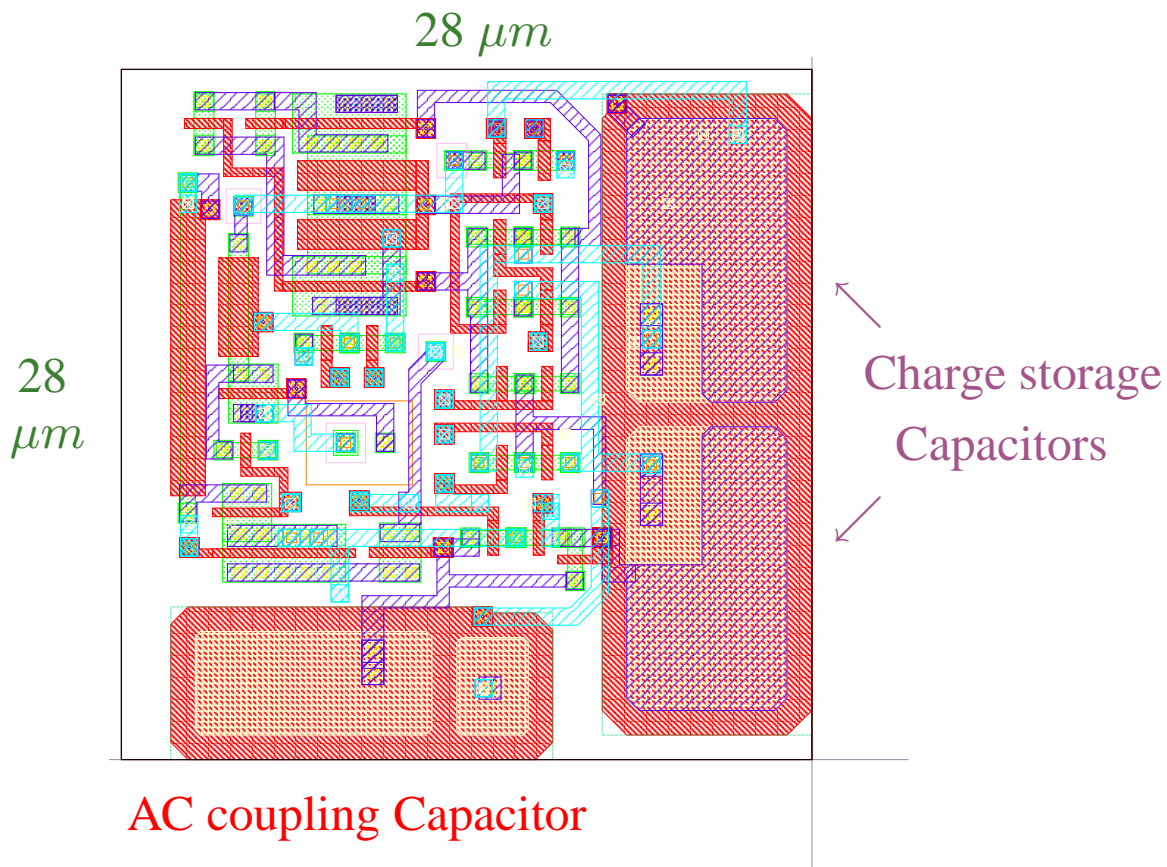
♣ IReS-LEPSI / DAPNIA collab.

♣ back from foundry: tests starting in Strasbourg and Saclay

⇒ first results in February-March 2003

MIMOSA-6 pixel layout

- Correlated double sampling integrated on $28 \times 28 \mu\text{m}^2$ pixels (designed by IReS - LEPSI)



1. charge stored in transistor connected to n-well is amplified
2. amplified charge is stored in 1st capacitor
3. amplified charge stored in 2nd capacitor (previous event) is subtracted from charge in 1st capacitor
4. result is sent to end of column for discrimination
5. charge is read again, amplified and stored in 2nd capacitor